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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,171	02/01/2002	Brian Samuel Beaman	YOR919960186US2	3582

7590 08/17/2010

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EXAMINER	
LEADER, WILLIAM T	
ART UNIT	PAPER NUMBER
1795	

MAIL DATE	DELIVERY MODE
08/17/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/066,171	BEAMAN ET AL.	
	Examiner	Art Unit	
	WILLIAM T. LEADER	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *49-60 and 66-114* is/are pending in the application.

4a) Of the above claim(s) *50-60,67-80,82-85,87,89,95 and 97-102* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49,66,81,86,88,90-94,96 and 103-114* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt of the papers filed on June 1, 2010, is acknowledged. Applicant has elected Group I without traverse. At page 12 of the response, applicant states that claim 94 has been amended to be in method form and is now part of elected Group I.

Claim Objections

2. Claims 104, 106 and 107 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Independent claim 49, on which claims 105 directly or indirectly depend, has been amended to recite that there is an exposed portion of the elongated electrical conductor "at the second end" that is not coated with the dielectric coating. Claims 104, 106 and 107 recite the exposed portion is at "the second end". Since claim 49 now recites that the exposed portion is at the second end, claims 104, 106 and 107 do not further limit claim 49.

3. Applicant is advised that should claims 105 and 108 be found allowable, claim 108 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 49, 81, 90, 91, 96, 103, 104 and 106 are rejected under 35 U.S.C. 102(e) as being anticipated by Eldridge et al (US 6,110,823).

6. The Eldridge et al patent (hereinafter Eldridge) is directed to a method for forming contact structures. The contact structures are formed by bonding a free end of a wire to a substrate, and subsequently overcoating the wire with a least one layer of material. See the abstract. The contact structures of Eldridge may be used as probes (column 14, lines 25-32). Thus, Eldridge is directed to the same field of endeavor as applicant's invention which, as indicated in the title, is directed to methods of fabrication of probe structures.

7. Figures 5 of Eldridge illustrates a wire which has been coated with at least two layers of material to create a resilient contact structure (column 16, lines 15-18). Wire 502 has a first (proximal) end and a second (distal) end. The first end is bonded to terminal 512 (column 46, lines 55-63). This corresponds to the "providing" and "bonding" steps of claim 49. Figure 5 shows conductor 502 coated with inner coating layer 520 and outer coating layer 522. Eldridge teaches that the outermost (top) layer or both layers is/are a conductive material (column 47, lines 15-18; lines 38-39). This clearly indicates that the inner layer may be other than a

conductive material, i.e., a dielectric material. Eldridge additionally teaches coating a dielectric layer onto a wire in the embodiment of figure 10k which includes a layer of dielectric material 1094 (column 67, lines 55-59). This corresponds to the "forming a dielectric coating" step of claim 49. Eldridge teaches that generally, the vertical end portions (as illustrated) of the wire stem do not contribute to the overall resiliency of the contact structure. The coating need not cover the second end which may be exposed as shown in figure 5B (column 48, lines 16-29). As indicated in the abstract and column 1, lines 26-42, the method is for forming a plurality of connections. All limitations recited in independent claim 49 are taught by Eldridge et al.

8. With respect to claims 81, Eldridge et al shows in several figures, including figures 5, 5b and 10k, that the conductor has a shape which is partially curved and partially linear.

9. With respect to claim 90, Eldridge et al discloses that the resilient contact structures may be used as probes (column 14, lines 28-29). A resilient and/or compliant (springy) contact structure which is securely mounted to an electronic component may be used for effecting temporary connection of the electronic component to another electronic component (column 12, lines 43-47). The resilient contact structures can be used to temporarily connect an electronic component for procedures such as burn-in and testing of the electronic component (column 14, lines 44-47).

10. With respect to claim 91, Eldridge et al discloses that it is known to utilize a test device with a plurality of wires in high density PCB and IC (integrated circuit) testing applications (column 5, lines 1-11).

11. With respect to claim 96, figures 5 and 5b of Eldridge et al shows conductor 502 with first end 502a bonded to a terminal 512 on substrate 508. The second end is formed with ball

(protuberance) 534. See column 46, lines 55-62. This ball is a protuberance as recited in claim 96.

12. With respect to claim 103, the figures of Eldridge indicate that the coating is conformal and substantially uniform.

13. Claims 104 and 106 recite that the exposed portion is at the second end. This limitation is also present in independent claim 49 on which claims 104 and 106 directly or indirectly depend, and is discussed above.

Claim Rejections - 35 USC § 103

14. Claims 49, 81, 90, 91, 96, 103, 104 and 106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (US 6,110,823).

15. For the reasons given above, Eldridge is considered to teach all limitations of independent claim 49 and dependent claims 81, 90, 91, 96, 103, 104 and 106. Eldridge discloses both forming a dielectric coating and forming a conductor that is exposed at the second end. There is no requirement that all embodiments suggested by a reference be illustrated. A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art. MPEP 2123 I. The teachings of a reference are not limited to merely that which is set forth in the examples. Instead "[a] reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art", and *In re Widmer*, 147 USPQ 518, 523 (CCPA 1965). As noted, Eldridge teaches that that generally, the vertical end portions of the wire stem do not contribute to the overall resiliency of the contact structure

(column 48, lines 16-29). In view of this teaching it would have been at least obvious to have omitted all coating from the second end (distal vertical end as illustrated) of the conductor.

16. Claims 66, 105 and 108-114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (US 6,110,823) in view of Saruwatari et al (US 5,233,011).

17. Claim 66 differs from Eldridge et al by reciting specific materials from which the dielectric layer is formed. The Saruwatari et al patent is directed to a process for preparing an insulated wire. The insulation is made from a polyimide. See the abstract. Aromatic polyimide has excellent mechanical properties, solvent resistance, electrical insulative properties, and the highest thermal resistance among organic polymers. See column 1, lines 18-22. Claims 105 and 108-114 recite that the dielectric coating does not contain a metal constituent. Polyimide is a polymer made from atoms of carbon, hydrogen, oxygen and nitrogen, and does not contain a metal constituent. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have formed the dielectric insulation around the conductors of Eldridge from polyimide because polyimide has excellent mechanical and electrical properties as taught by Saruwatari et al.

18. Claims 86, 88, 92, 93, 94 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (US 6,110,823) in view of Nakata et al (US 5,665,610).

19. Eldridge et al recognizes that modern integrated circuits are generally produced by creating several, typically identical, integrated circuit dies on a single semiconductor wafer (column 73, lines 1-4). "Burn-in" is a process whereby a chip (die) is either simply powered up

or is powered up and signals exercising to some degree the functionality of the chip are applied. It is known to perform burn-in prior to singulating the dies. Typically, the temporary connections to the dies are made by test probes or by "flying wires". See column 73, lines 15-26.

20. Claim 86 differs from Eldridge et al by reciting that the plurality of conductors are distributed into a plurality of groups, while claim 88 recites that the groups are arranged in an array. Claim 92 recites the groups correspond to integrated circuit chips on a substrate and claim 93 recites a plurality of integrated circuit chips. The Nakata et al patent is directed to a semiconductor device checking method. Nakata et al teach that in order to guarantee the quality of bare (unpackaged) chips, it is necessary to perform checks such as burn-in while the device is part of the wafer. Nakata et al recognize that it takes a long time to check a plurality of bare chips formed on the wafer one by one. Consequently, it is required that a check such as burn-in should be made on a plurality, for example, 1000 or more bare chips while the chips are part of the wafer. A supply voltage and a signal to the check electrodes of a plurality of semiconductor chips formed on the wafer are simultaneously applied so as to operate the chips. It is necessary to prepare a probe card having a large number of probe terminals. See column 1, lines 27-46. Figure 3 shows an example of a semiconductor wafer housing for causing bump15 of the contactor 14 to come in contact with the check electrode 11 of the semiconductor chip 10. See column 5, lines 41-44. As illustrated in figure 3(a) and 3(b), bumps 15 are distributed in a plurality of groups of four which form an array. It would have been obvious at the time the invention was made to have formed the plurality of conductors in Eldridge into an array of

groups as illustrated by Nakata et al because it would have facilitated testing each chip of a plurality of chips on a single wafer.

21. Claim 94 recites holding the substrate for retractably moving the substrate toward an electronic device and applying electrical signals to the conductors. Nakata et al disclose that in figures 3(a) and 3(b) element 21 is a holding plate for holding semiconductor wafer A. As shown in the figures, contactor 14 is adapted to be brought into contact with wafer A. See column 5, lines 45-54. As noted above, signals are supplied to the check electrodes so as to operate the chips. It would have been obvious at the time the invention was made to have provided a housing for retractably moving the substrate toward the conductors of Eldridge in a testing procedure as taught by Nakata et al because temporary contact with the wafer being tested would have been obtained.

22. Claim 107 recites that the exposed portion is at the second end. This limitation is also present in claim 49 on which claim 107 indirectly depends, and is discussed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM T. LEADER whose telephone number is (571) 272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick J. Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William Leader/
August 13, 2010

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